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(54) INTEGRATED CIRCUIT DEVICE METHODS AND MODELS WITH PREDICTED DEVICE METRIC VARIATIONS

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See application file for complete search history.

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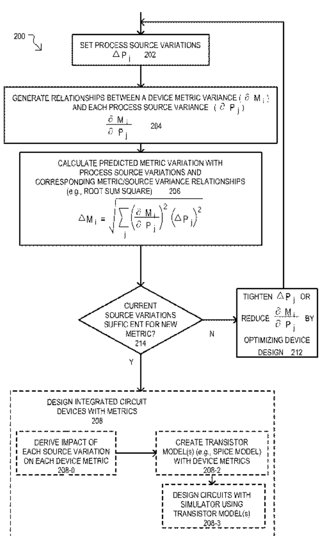
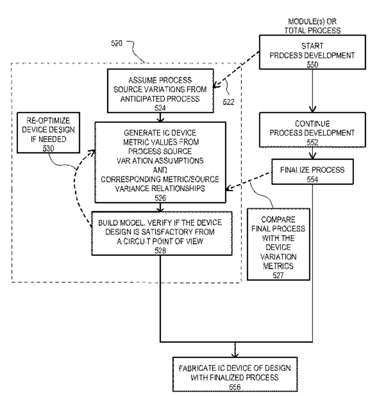
(57) **ABSTRACT**

A method can include selecting integrated circuit (IC) device fabrication process source variations; generating relationships between each process source variance and a device metric variance; and calculating at least one IC device metric value from the process source variations and corresponding relationships between each process source variance and a device metric variance.

12 Claims, 9 Drawing Sheets





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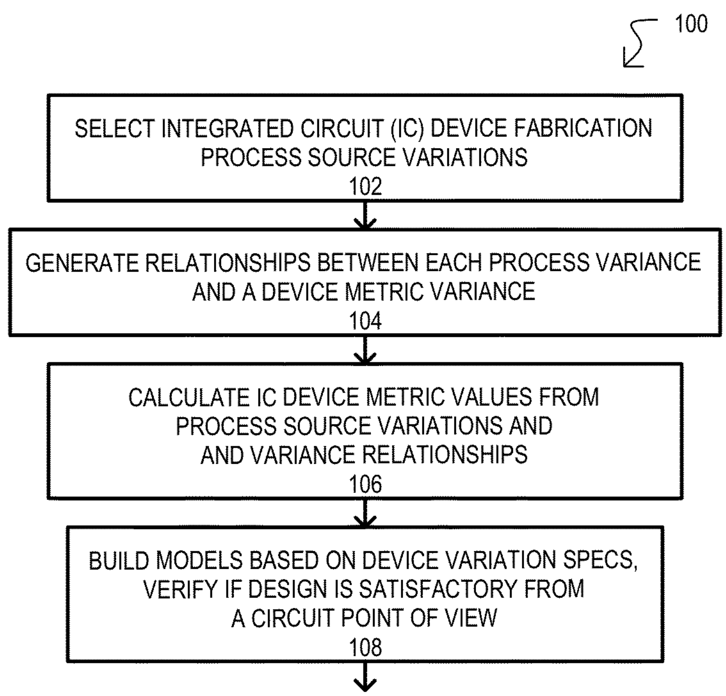

100
SELECT INTEGRATED CIRCUIT (IC) DEVICE FABRICATION PROCESS SOURCE VARIATIONS
102
GENERATE RELATIONSHIPS BETWEEN EACH PROCESS VARIANCE AND A DEVICE METRIC VARIANCE
104
CALCULATE IC DEVICE METRIC VALUES FROM PROCESS SOURCE VARIATIONS AND AND VARIANCE RELATIONSHIPS
106
BUILD MODELS BASED ON DEVICE VARIATION SPECS, VERIFY IF DESIGN IS SATISFACTORY FROM A CIRCUIT POINT OF VIEW
108

FIG. 1

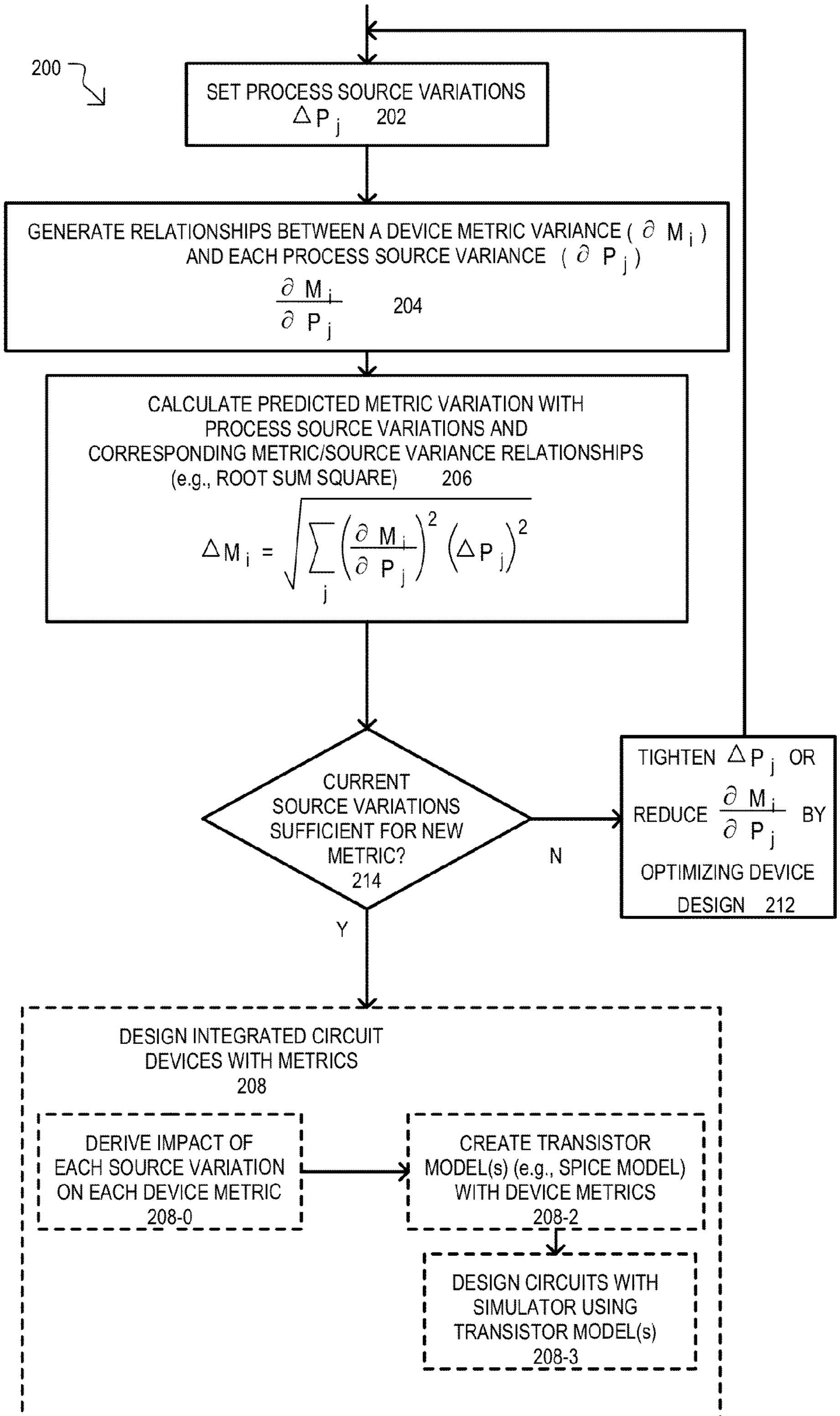

200
SET PROCESS SOURCE VARIATIONS
ΔP_j 202
GENERATE RELATIONSHIPS BETWEEN A DEVICE METRIC VARIANCE (∂M_i) AND EACH PROCESS SOURCE VARIANCE (∂P_j)
$\frac{\partial M_i}{\partial P_j}$ 204
CALCULATE PREDICTED METRIC VARIATION WITH PROCESS SOURCE VARIATIONS AND CORRESPONDING METRIC/SOURCE VARIANCE RELATIONSHIPS (e.g., ROOT SUM SQUARE) 206
$\Delta M_i = \sqrt{\sum_j \left(\frac{\partial M_i}{\partial P_j}\right)^2 \left(\Delta P_j\right)^2}$
CURRENT SOURCE VARIATIONS SUFFICIENT FOR NEW METRIC? 214
N
Y
TIGHTEN ΔP_j OR REDUCE $\frac{\partial M_i}{\partial P_j}$ BY OPTIMIZING DEVICE DESIGN 212
DESIGN INTEGRATED CIRCUIT DEVICES WITH METRICS
208
DERIVE IMPACT OF EACH SOURCE VARIATION ON EACH DEVICE METRIC
208-0
CREATE TRANSISTOR MODEL(s) (e.g., SPICE MODEL) WITH DEVICE METRICS
208-2
DESIGN CIRCUITS WITH SIMULATOR USING TRANSISTOR MODEL(s)
208-3

FIG. 2

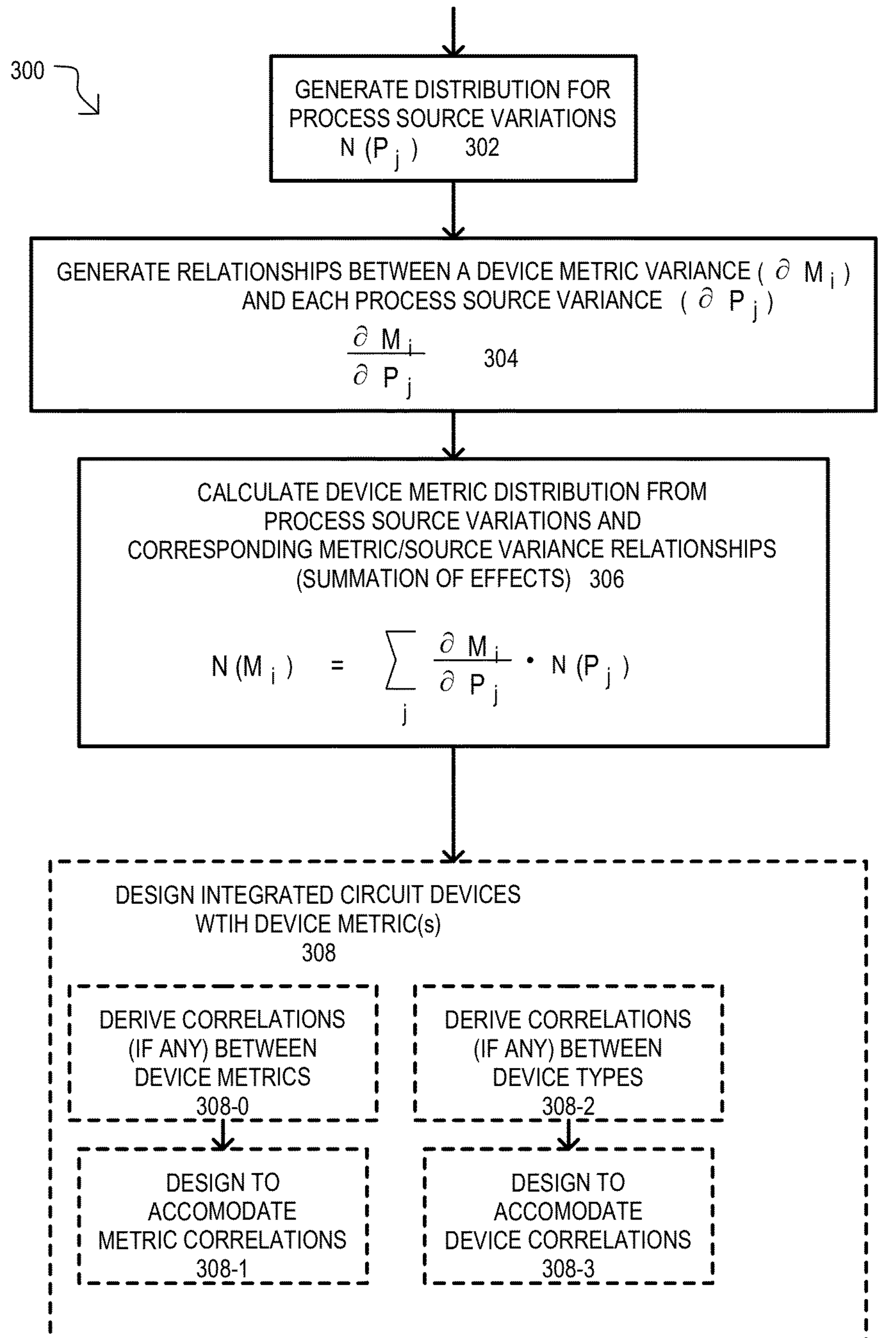
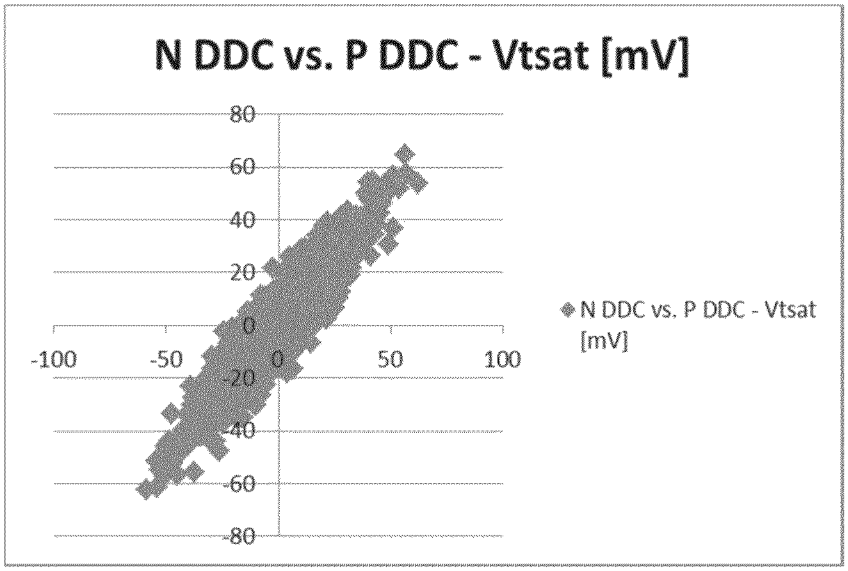
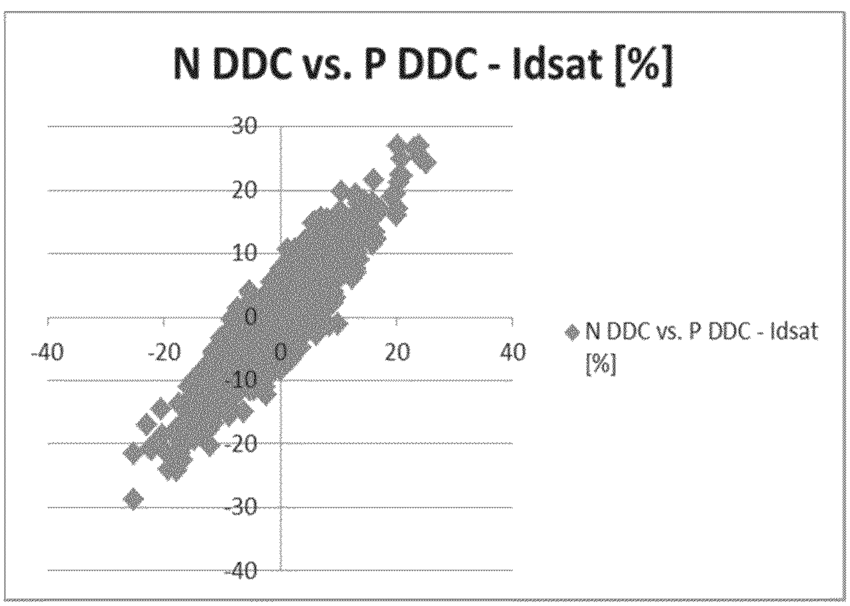

300
GENERATE DISTRIBUTION FOR PROCESS SOURCE VARIATIONS $N(P_j)$ 302
GENERATE RELATIONSHIPS BETWEEN A DEVICE METRIC VARIANCE (∂M_i) AND EACH PROCESS SOURCE VARIANCE (∂P_j)
$\frac{\partial M_i}{\partial P_j}$ 304
CALCULATE DEVICE METRIC DISTRIBUTION FROM PROCESS SOURCE VARIATIONS AND CORRESPONDING METRIC/SOURCE VARIANCE RELATIONSHIPS (SUMMATION OF EFFECTS) 306
$N(M_i) = \sum_j \frac{\partial M_i}{\partial P_j} \cdot N(P_j)$
DESIGN INTEGRATED CIRCUIT DEVICES WTIH DEVICE METRIC(s) 308
DERIVE CORRELATIONS (IF ANY) BETWEEN DEVICE METRICS 308-0
DERIVE CORRELATIONS (IF ANY) BETWEEN DEVICE TYPES 308-2
DESIGN TO ACCOMODATE METRIC CORRELATIONS 308-1
DESIGN TO ACCOMODATE DEVICE CORRELATIONS 308-3

FIG. 3A



correlation: 0.926

FIG. 3B



correlation: 0.917

FIG. 3C

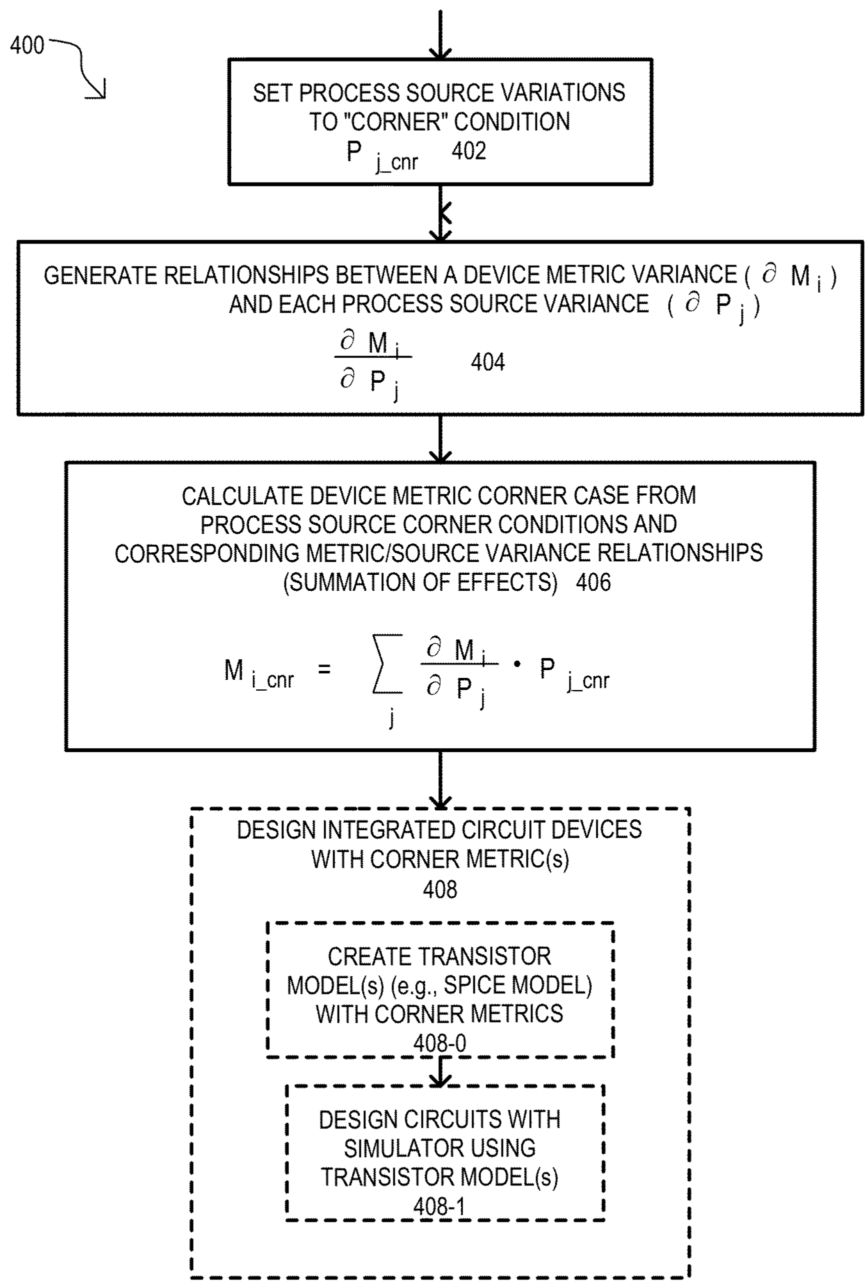

400
SET PROCESS SOURCE VARIATIONS
TO "CORNER" CONDITION
P_{j_cnr} 402
GENERATE RELATIONSHIPS BETWEEN A DEVICE METRIC VARIANCE (∂M_i)
AND EACH PROCESS SOURCE VARIANCE (∂P_j)
$\frac{\partial M_i}{\partial P_j}$ 404
CALCULATE DEVICE METRIC CORNER CASE FROM
PROCESS SOURCE CORNER CONDITIONS AND
CORRESPONDING METRIC/SOURCE VARIANCE RELATIONSHIPS
(SUMMATION OF EFFECTS) 406
$M_{i\_cnr} = \sum_j \frac{\partial M_i}{\partial P_j} \cdot P_{j\_cnr}$
DESIGN INTEGRATED CIRCUIT DEVICES
WITH CORNER METRIC(s)
408
CREATE TRANSISTOR
MODEL(s) (e.g., SPICE MODEL)
WITH CORNER METRICS
408-0
DESIGN CIRCUITS WITH
SIMULATOR USING
TRANSISTOR MODEL(s)
408-1

FIG. 4

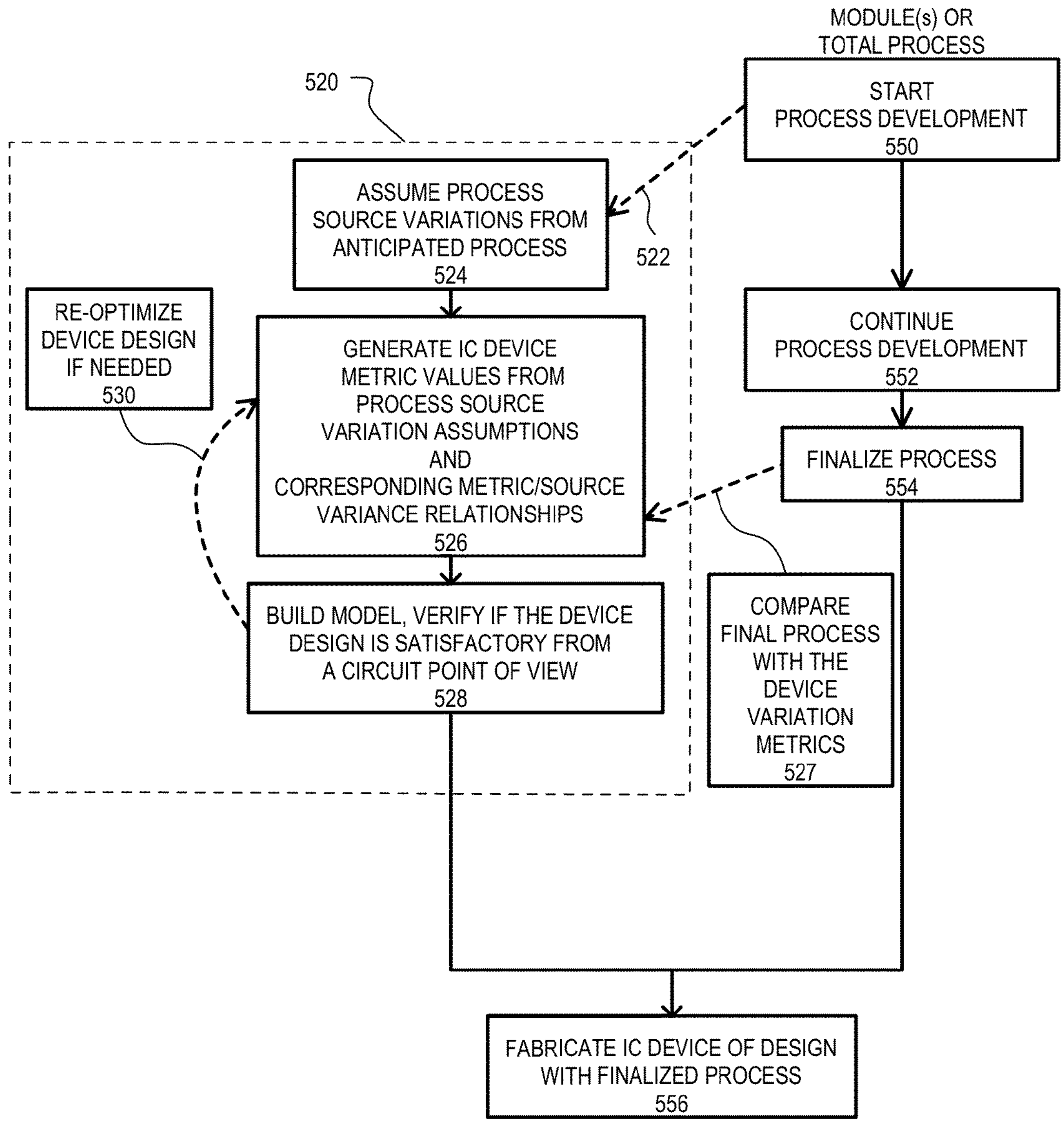

MODULE(s) OR
TOTAL PROCESS
START
PROCESS DEVELOPMENT
550
520
ASSUME PROCESS
SOURCE VARIATIONS FROM
ANTICIPATED PROCESS
524
522
RE-OPTIMIZE
DEVICE DESIGN
IF NEEDED
530
GENERATE IC DEVICE
METRIC VALUES FROM
PROCESS SOURCE
VARIATION ASSUMPTIONS
AND
CORRESPONDING METRIC/SOURCE
VARIANCE RELATIONSHIPS
526
CONTINUE
PROCESS DEVELOPMENT
552
FINALIZE PROCESS
554
BUILD MODEL, VERIFY IF THE DEVICE
DESIGN IS SATISFACTORY FROM
A CIRCUIT POINT OF VIEW
528
COMPARE
FINAL PROCESS
WITH THE
DEVICE
VARIATION
METRICS
527
FABRICATE IC DEVICE OF DESIGN
WITH FINALIZED PROCESS
556

FIG. 5

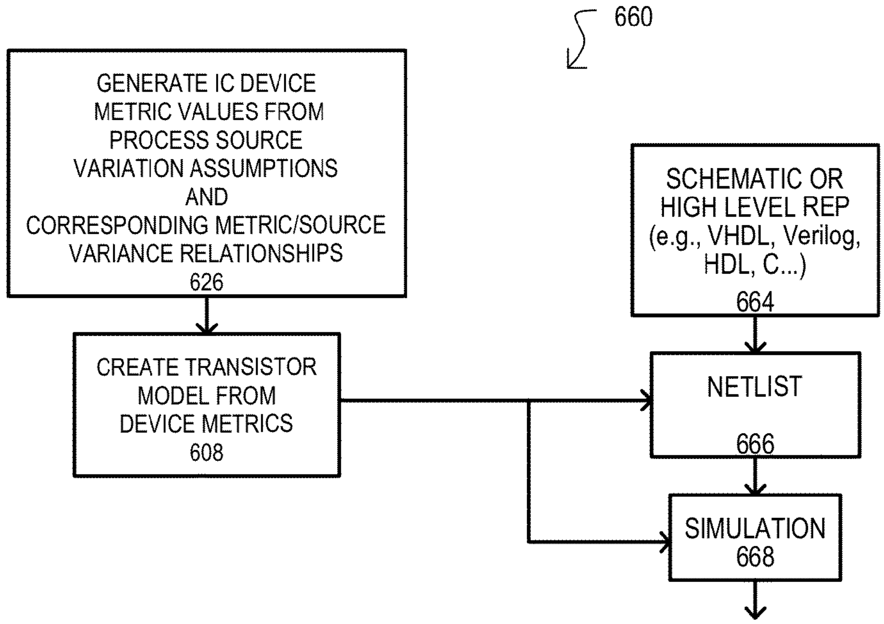

660
GENERATE IC DEVICE METRIC VALUES FROM PROCESS SOURCE VARIATION ASSUMPTIONS AND CORRESPONDING METRIC/SOURCE VARIANCE RELATIONSHIPS 626
CREATE TRANSISTOR MODEL FROM DEVICE METRICS 608
SCHEMATIC OR HIGH LEVEL REP (e.g., VHDL, Verilog, HDL, C...) 664
NETLIST 666
SIMULATION 668

FIG. 6

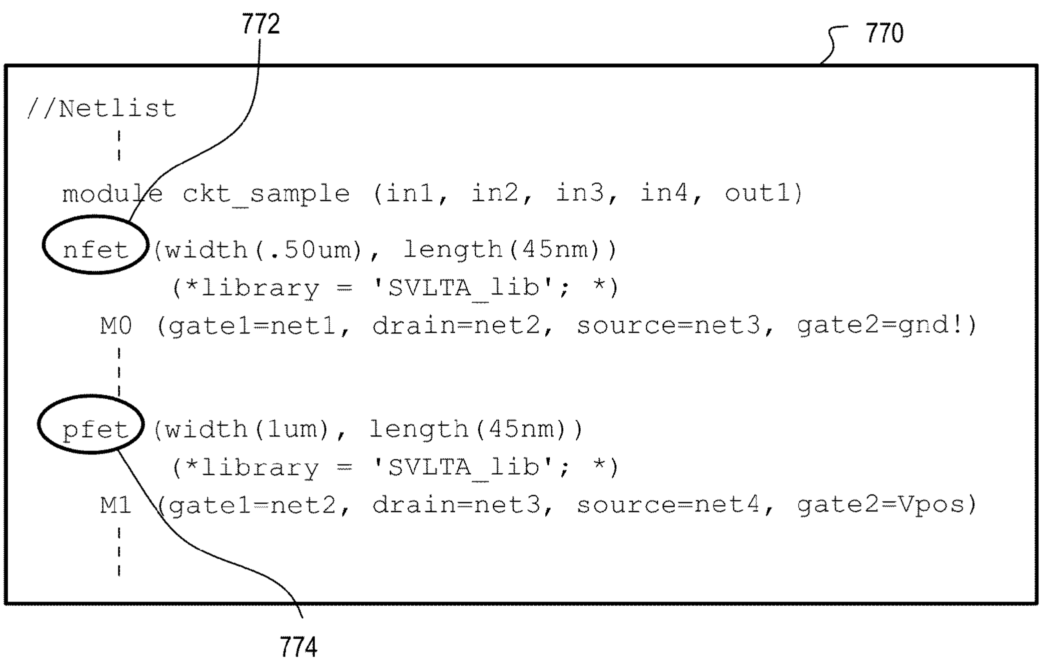

772
770
//Netlist
module ckt_sample (in1, in2, in3, in4, out1)
nfet (width(.50um), length(45nm))
(*library = 'SVLTA_lib'; *)
M0 (gate1=net1, drain=net2, source=net3, gate2=gnd!)
pfet (width(1um), length(45nm))
(*library = 'SVLTA_lib'; *)
M1 (gate1=net2, drain=net3, source=net4, gate2=Vpos)
774

FIG. 7

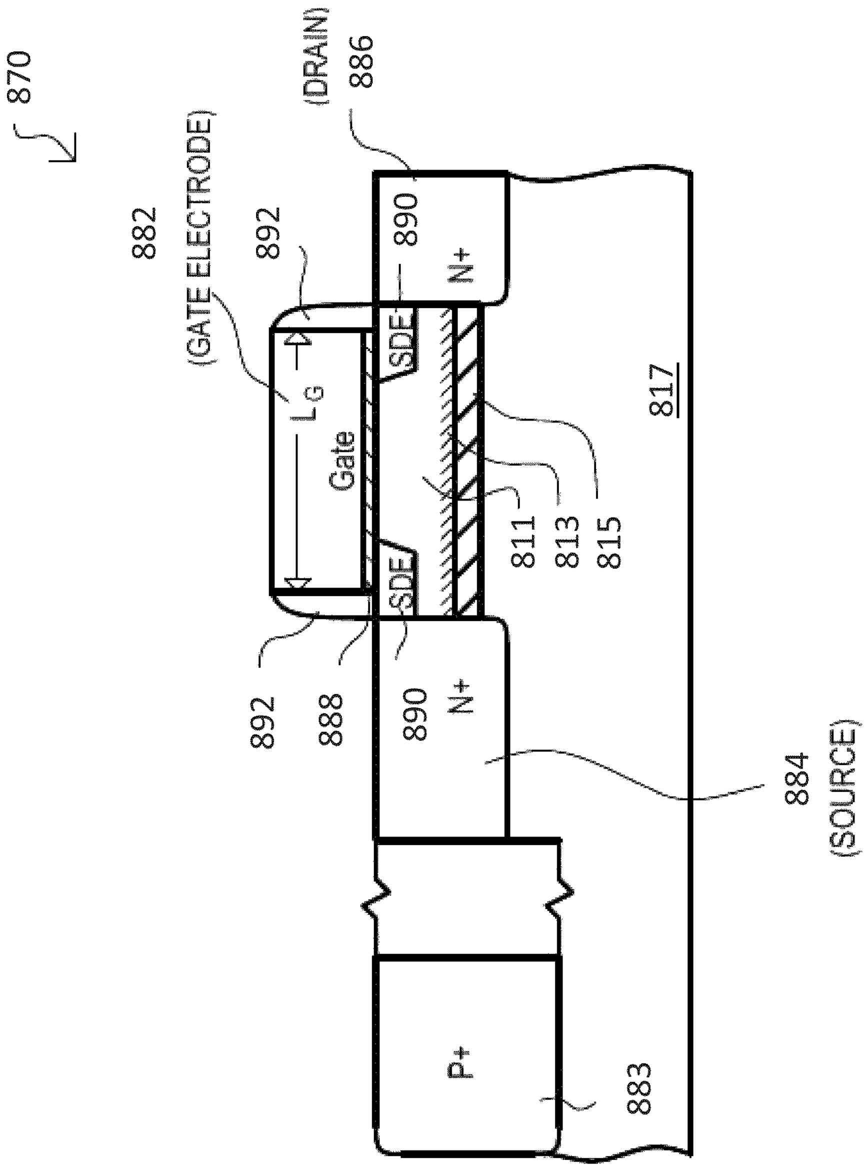

870
882
(GATE ELECTRODE)
892
886
(DRAIN)
890
N+
SDE
LG
Gate
SDE
892
888
890
N+
811
813
815
817
884
(SOURCE)
P+
883

FIG. 8A

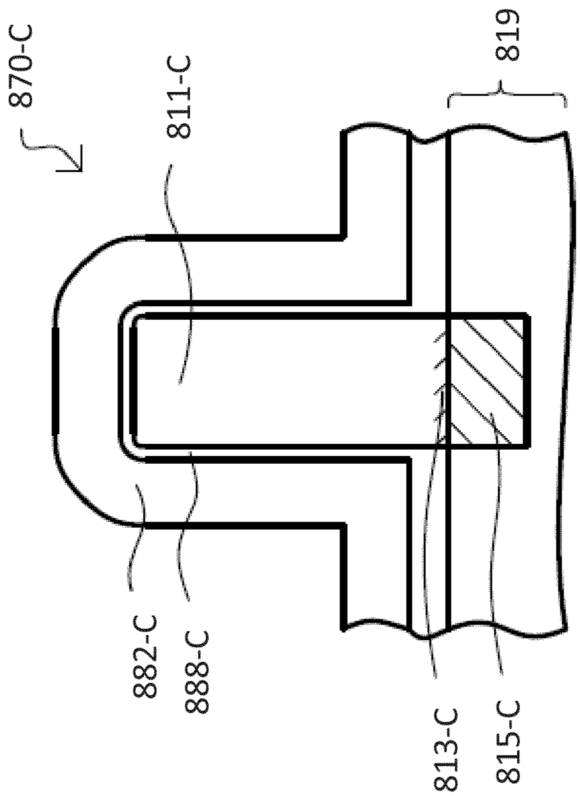


FIG. 8C

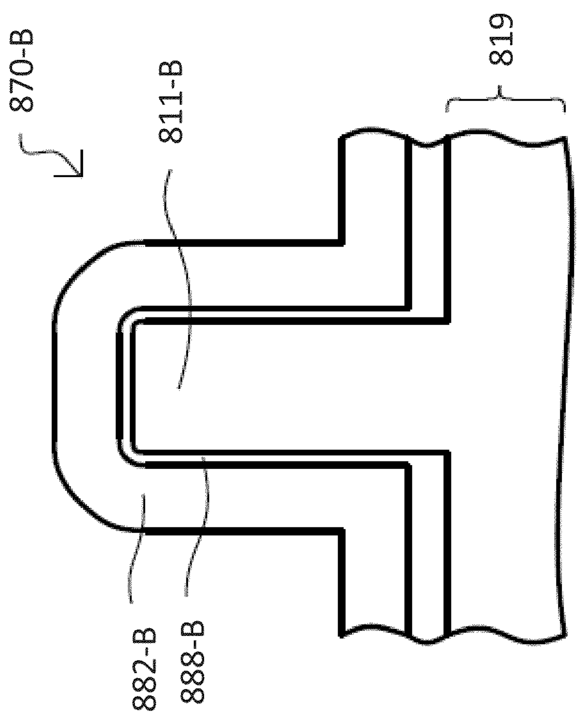


FIG. 8B

INTEGRATED CIRCUIT DEVICE METHODS AND MODELS WITH PREDICTED DEVICE METRIC VARIATIONS

TECHNICAL FIELD

This disclosure relates generally to integrated circuit design and modeling, and more particularly to generating predicted device performance metrics from assumed variations in fabrication process steps or results.

BACKGROUND

Conventional integrated circuit (IC) design methods utilize "hardware-based" approaches to predict device metrics (such as transistor performance metrics). For example, performance data can be collected from various dies on a number of fabricated wafers and then analyzed. Based on such analysis, models (e.g., transistor models) can then be created, which can serve as basis for simulating circuit behavior.

Such conventional approaches can suffice for mature fabrication processes. However, for processes still under development, such hardware data is generally unreliable as fabrication steps can be subject to change or the fabrication process drifts, making the initial metrics inaccurate thereby necessitating multiple rounds of design as the circuit behaviors evolve with the progression of the process development. Also, conventional approaches may only present performance data, making it difficult to obtain comprehensive information on how the sources of particular process variations can impact different device metrics.

Fabricated IC devices tend to encounter failures or underperforming components due to fabrication process variations, for instance, variations in threshold voltage. As a result, designers may elect to design conservatively, that is, to a wider set of process corners for the sake of ensuring a robust design but then sacrificing certain design targets. As semiconductor process advances to support Moore's law, the challenges of designing ICs in the context of process development only increase as the processes become more complex and therefore difficult to develop and implement. Design compensations for the ever-widening corners only increase. The trend continues with putting more and more burdens on design teams to tape out new chip products with satisfactory designs and meeting timelines for customers.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1** is a flow diagram of a method according to an embodiment.

FIG. **2** is a flow diagram of a method according to another embodiment.

FIG. **3**A is a flow diagram of a method according to a further embodiment.

FIGS. **3**B and **3**C are graphs showing derived correlations between device metrics according to very particular embodiments.

FIG. **4** is a flow diagram of a method according to a further embodiment.

FIG. **5** is a flow diagram of a method according to a further embodiment.

FIG. **6** is a flow diagram of a method according to an additional embodiment.

FIG. **7** is a diagram of a model and model elements according to an embodiment.

FIGS. **8**A to **8**C are diagrams of transistors for which device metrics can be generated, according to various embodiments.

DETAILED DESCRIPTION

Various embodiments of the present invention will now be described in detail with reference to a number of drawings. The embodiments show methods to generate predicted integrated circuit (IC) device metrics from assumed process variations, to reliably model circuit behaviors in circuit simulators (e.g., SPICE) even during the course of a fabrication process that is in-development. Embodiments can enable designs by way of utilizing statistically derived relationships between metrics and/or process variations, including but not limited to: the impact of individual source variations on each device metric; correlations between different device metrics; and correlations between different device types.

FIG. **1** shows a method **100** according to an embodiment. A method **100** can include selecting IC device fabrication process source variations (**102**). Process source variations usually refer to process targets relevant to behavior of fabricated components that can vary based upon variation of corresponding fabrication process steps. Note that while process source variations can include front-end processes for active (i.e., transistor) and passive (e.g., resistor, varactors) device fabrication, such values can also include variations resulting other process steps, including but not limited to interconnect metallization process steps or back-end processes (e.g., interconnect and/or packaging steps and/or variations).

In very particular embodiments, the process source variations can include transistor related source variations, including but not limited to: gate length (Lgate); gate insulator thickness (Tox); effective channel width (Weff); ion implantation energy and dose for threshold voltage adjustment (Vt dosage); Halo (or pocket)-implant dose; lightly doped drain (LDD) ion implant dose; transistor spacer thickness; and other fabrication steps targeting specific dimensions or concentrations and profiles to achieve a pre-selected transistor design. In addition or alternatively, source variations can include interconnect related variations that could impact other aspects of a resulting circuit, including but not limited to: chemical mechanical polishing (CMP) planarization; via and interlayer dielectric (ILD) thickness; interconnect metal thickness; interconnect metal width; via and contact size; and other fabrication steps specific to creating pre-selected structures to achieve pre-selected circuit elements with interconnected transistors. Still further, process source variations can include package related variations, including but not limited to: wiring inductance; wiring resistance; and pad-bond resistance.

It is understood that these listed values are provided by way of example only. Any suitable IC production effects can be included as a process source variation.

While the process source variation are described herein in reference to transistor structures and in particular, MOS type field effect transistors (FETs), alternate embodiments can include process source variation for other device types, including but not limited to bipolar junction transistors, junction FETs, finFETs or any other suitable active device.

In some embodiments, process source variations can be assumed from the expected fabrication process.

A method **100** can also include generating relationships between each process variance and a device metric variance (**104**). Such an action can include generating a value that reflects the extent to which each selected process source variations can affect a desired device metric. Such a relationship value can be expressed as the derivative of metric variance to source variance (∂M/∂P). In general, the relationship values for given process source variations can be extracted using one or more Technology Computer Aided Design (TCAD) tools.

Device metric values can represent any suitable IC device performance characteristic. In very particular embodiments, the device metric values are for representative transistor behaviors, including but not limited to: linear region threshold voltage (Vtlin), linear region drain current (Idlin); saturation region threshold voltage (Vtsat); drain induced barrier lowering (DIBL) effect; saturation drain current (Idsat); subthreshold swing at saturation (Sssat); effective drain current (Ieff); gate capacitance (Cgg); and overlap capacitance (Cov) for a given transistor design and type. In addition or alternatively, device metrics can include interconnect related parameters, including but not limited to: via resistance (Rvia); interlevel capacitance (capacitance between lines of different layers, Ginter); and intra-level capacitance (capacitance between lines of same layer, Cintra).

Method **100** further includes calculating IC device metric specification values from the process source variations and the variance relationships (**106**). Such a calculation preferably uses a root-sum square mathematical formula as follows:

$$\Delta M_i = \sqrt{\sum_j \left(\frac{\partial M_i}{\partial P_j}\right)^2 (\Delta P_j)^2}$$

Where $\partial M_i/\partial P_j$ is the derivative relationship between device metric value in relation to given process, for instance, the device metric of threshold voltage as affected by threshold voltage-setting implant condition, and can generally be obtained by a pre-modeled computer program such as technology computer aided design (TCAD); and ΔP_j represents each of the sources of process variations affecting the behavior of the fabricated transistor, for instance, drawn gate-length, thickness of gate dielectric, etc.

Once the calculation is performed and the device metric value ΔM_i is obtained for a given set of conditions, the device metric value can be used to create transistor models **108** for circuit simulation for verifying circuit designs, for instance, in SPICE. The device metric value ΔM_i is preferably determined for various process variation cases, so that the calculated device metric value ΔM_i represents the middle as well as device corner values. Calculated device metric values can therefore be used to for simulation models to enable evaluation of circuit designs, or can be used with existing circuit designs to evaluate the transistor device design itself, and can enable the evaluation of the semiconductor process from which the process source variations are obtained, all using modeling techniques, thereby alleviating the need to run large amounts of silicon wafers.

FIG. **2** is a flow diagram of a method (**200**) according to a further embodiment. A method **200** can include providing process source variations (ΔP_j) (**202**). Process source variations (ΔP_j) normally have a Gaussian distribution and the sigma values of the distributions can be obtained from the fabrication process assumptions.

Method **200** can include generating relationships between a device metric variance and each corresponding process source variance ($\partial M_i/\partial P_j$) (**204**). In general, variance relationships ($\partial M_i/\partial P_j$) can be extracted from a tool, such as TCAD, as but one example.

Method **200** then calculates a metric variation (ΔM_i) with the selected process source variations and corresponding variance relationships (**206**), preferably by applying the root sum of squares formula at **206**. Method **200** can then proceed to a checkpoint to determine if the input current process source variations are sound, in other words, sufficient to calculate a next device metric variation (Y from **214**). Such an action can be based on a check of a calculated device metric ΔM_i against a predetermined set of target device metrics. If the process source variations are sufficient, then method **200** returns to box **204** to generate new variance relationships to calculate another device metric. If the current process source variations are not sufficient to calculate a next device metric variation (N from **214**), a method **200** can return to box **202** to setup data values **212** for the process source variations necessary to generate the new device metric variation.

Once all desired device metrics have been generated (Y from **210**), an integrated circuit device can be designed using the predicted device metric variations **208**. It is understood that then, any suitable design steps can be taken from the predicted device metric variations.

As one example of an implementation of the process of FIG. **2**, there is generated at Table 1 a set of parameters for ∂M_i and for ∂P_j for an exemplary DDC transistor (further described below) in a 28 nm process node for a nominal drawn gate length of 36 nm. Example process variations sources identified are, L (gate length), Tox (gate oxide thickness), ΔEpi (epitaxial layer) thickness, ΔScreen D dose (further described below), LDD D (source/drain extension) implant dosage, Spacer 1 (first sidewall spacer) thickness, Spacer 2 (second sidewall spacer) thickness, and W (FET channel width). Related and corresponding device metrics include Vtlin, Idlin, Vtsat, DIBL, Idsat, SSat, Ieff, Cgg and Coy (all described above).

TABLE 1

	Process Variation Source (σP_j)							
σM_i	L [/nm]	Tox [/Å]	ΔEpi [/Å]	ΔScreen D: [/%]	LDD D [/%]	Spacer 1 [/nm]	Spacer 2 [/nm]	*W [/nm]
Vtlin [mV/]	8.80	22.00	3.20	−2.80	−0.50	22.00	0.50	0.07
Idlin [%/]	−1.60	−5.80	−0.82	0.68	0.29	−16.30	−0.28	0.17
Vtsat [mV/]	12.80	18.00	3.70	−3.00	−0.60	32.00	1.00	0.07
DIBL [mV/]	−4.00	4.00	−0.50	0.20	0.10	−10.00	−0.50	0.00
Idsat [%/]	−3.46	−8.70	−1.37	1.02	0.34	−19.20	−0.36	0.17
SSsat [mV/]	−0.21	1.44	0.07	−0.02	0.02	−0.75	0.00	0.00
Ieff [%/]	−4.10	−10.90	−1.61	1.27	0.36	−20.00	−0.38	0.17
Cgg [%/]	1.50	−2.80	−0.02	0.01	0.01	−1.90	0.03	0.17
Cov [%/]	−0.14	−0.66	−0.11	0.05	0.06	−6.55	0.03	0.17
Vtlin [mV/]	8.80	22.00	3.20	−2.80	−0.50	22.00	0.50	0.07

The derived numbers above, as well as estimated ΔP_j are then used in the process at Step **206** to result in device metric variations calculated as a root sum square value. An example of a result of applying Step **206** is at Table 2 below.

TABLE 2

	Process Variation Source (ΔP_j)								
ΔM_i	ΔL: 2 nm	ΔTox: 7Å	ΔEpi: 10Å	ΔScreen D: 5%	ΔLDD D: 5%	ΔSpacer 1: 0.6 nm	ΔSpacer 2: 2 nm	*ΔW: 5 nm	Total (RSS)
Vtlin [mV]	17.60	15.40	16.00	−28.00	−2.50	13.20	1.00	0.34	42.05
Idlin [%]	−3.20	−4.06	−4.10	6.80	1.45	−9.78	−0.56	0.83	13.73
Vtsat [mV]	25.60	12.60	18.50	−30.00	−3.00	19.20	2.00	0.34	49.38
DIBL [mV]	−8.00	2.80	−2.50	2.00	0.50	−6.00	−1.00	0.00	10.92
Idsat [%]	−6.92	−6.09	−6.85	10.20	1.70	−11.52	−0.72	0.83	19.31
SSsat [mV]	−0.42	1.01	0.36	−0.15	0.09	−0.45	0.01	0.00	1.25
Ieff [%]	−8.20	−7.63	−8.05	12.70	1.80	−12.00	−0.76	0.83	22.36
Cgg [%]	3.00	−1.96	−0.09	0.09	0.04	−1.14	0.05	0.83	3.85
Cov [%]	−0.28	−0.46	−0.55	0.50	0.30	−3.93	0.06	0.83	4.13
Vtlin [mV]	17.60	15.40	16.00	−28.00	−2.50	13.20	1.00	0.34	42.05
Idlin [%]	−3.20	−4.06	−4.10	6.80	1.45	−9.78	−0.56	0.83	13.73
Vtsat [mV]	25.60	12.60	18.50	−30.00	−3.00	19.20	2.00	0.34	49.38
DIBL [mV]	−8.00	2.80	−2.50	2.00	0.50	−6.00	−1.00	0.00	10.92
Idsat [%]	−6.92	−6.09	−6.85	10.20	1.70	−11.52	−0.72	0.83	19.31
SSsat [mV]	−0.42	1.01	0.36	−0.15	0.09	−0.45	0.01	0.00	1.25

The calculated statistical device metric variations based upon process variations can be used to create a model, for instance, in SPICE, by which circuits can be simulated as part of the design process.

Device metric variations can be used to derive the impact of each source variation on each device metric **208-0**. With such information, an IC device or portion of such a device can be designed to take into account such high impact source variations **208-1**. In addition or alternatively, transistor models can be improved using the device metrics **208-2** derived from process variations. Based on the improved transistor models, the SPICE model can be improved. Circuits can then be designed using such improved transistor models **208-3**.

FIG. **3**A is a flow diagram of a method (**300**) according to another embodiment. A method **300** can include generating distributions for process source variations ($N(P_j)$) (**302**). In very particular embodiments, such distributions can be Gaussian distributions (with a median value of zero, and a 3-sigma variation based on sigma=$\Delta P_j/3$). Such a distribution can be generated in a manner like those described above (e.g., derived from initial fabrication process assumptions). Process source variations (ΔP_j) can include any of those described for embodiments herein, or equivalents.

A method **300** can then include generating relationships between a device metric variance and each corresponding to each process source variance ($\partial M_i/\partial P_j$) (**304**). Such relationships can be extracted from TOAD, for example.

A method **300** can then calculate a device metric distribution ($N(M_i)$) with the selected process source distributions and corresponding variance relationships ($\partial M_i/\partial P_j$) (**306**). In the embodiment shown, such an action can include generating a distribution of device metric values, each corresponding to a value from a process source distribution and the corresponding variance relationship ($\partial M_i/\partial P_j$). In particular embodiments, metric distributions $N(M_i)$ can be based on Gaussian distributions for process variations and the metric distributions can be derived using a Monte-Carlo statistical approach.

Once all desired device metric distributions have been generated, the device metric distributions can be used to facilitate circuit design **308**, for instance, to create a model for circuit simulation.

In the very particular embodiment shown, device metric distributions can be analyzed to determine correlations (if any) between device metrics **308-0**. In one very particular embodiment, such an action can include calculating a correlation coefficient between different distributions. For instance, the correlation between saturation threshold voltage or saturation drive current between transistor types (e.g., n-channel FETs and p-channel FETs) can be determined, as shown by example in FIGS. **3**B and **3**C for a 28 nm process node with drawn gate length of 36 nm.

With such information, a circuit can be designed with better accuracy with the correlations between devices understood **308-1**. The procedure of calculating correlations can be repeated for various metrics to further refine a circuit design **308-2** and **308-3**, for instance, by iterating on the choice of devices for the different nodes of a circuit.

FIG. **4** is a flow diagram of a method (**400**) according to another embodiment. A method **400** can include generating "corner" process source values (P_{j_cnr}) (**402**). Corner process source values can be values that lead to a device metric extreme. Thus, for each possible process source variation range (ΔP_j) it is known (or can be derived) which direction (e.g., leading to a 'faster' device or a 'slower' device than the nominal case) represents a corner condition for a given set of device metrics. Corner process source values (P_{j_cnr}) typically represent process parameter shifts to cause resulting devices to behave at the corners of the metric window.

A method **400** can include generating relationships between a device metric variance and its correspondence to each process source variance ($\partial M_i/\partial P_j$) (**404**), for which the process source variances can be extracted from a tool, such as TCAD for example. A method **400** can then calculate a corner device metric (M_{i_cnr}) for selected process source variances variance relationships to achieve device behavior at the corners (**406**).

Once all desired device metric corners have been generated, the device metrics can be used to facilitate circuit design based on corners **408**.

In the very particular embodiment shown, corner device metrics can be incorporated into transistor models of circuit simulators (e.g., SPICE models) and/or simulator operation **408-0**. Circuits can then be designed using such transistor models **408-1**. A benefit of this methodology is that device metric corner cases can be predicted based on process source variances and using models for correlating process source variances with device metrics. For instance, increased channel implant dosage results in a device having increased threshold voltage. When the methodology as embodied herein is used in the case of devices having reliable operating characteristics, and wherein the devices enjoy improved variation in threshold voltage, as well as stronger drive current and reduced DIBL, a SPICE model representing corners that are pulled-in from conventional windows can be created. Circuits can be simulated based upon the more aggressive SPICE model, thereby enabling greater options for circuit power, sizing, speed and other options.

FIG. **5** is a flow diagram of a method **520** according to another embodiment. A method **500** includes designing an IC device as a corresponding fabrication process is being developed. A method **520** includes assuming process source variations from expected fabrication process steps (**524**). Preferably, such assumptions can be made at the start of a fabrication process development **550**. A method **520** can generate IC device metric values from process source variation assumptions and corresponding metric/source variance relationships **526**, preferably by extracting the derivative relationship between device metric and process variation with a tool, such as TCAD. The device metrics values can then be used to make a preliminary circuit design **528**. It is noted that such actions can occur while a fabrication process is still being developed (e.g., **552**). The steps can go through iterative loops **530** to refine the device metrics based upon circuit simulations. The fabrication process development continues to proceed, using inputs from the device metric updates as necessary to compare against updates to device variation metrics **527**. When the process is finalized **554**, then a final set of device metric values can be calculated based upon a finalized set of process source variations **526**, using silicon data as necessary. The final device metric values are fed into circuit simulation models. Final refinements can be made to circuit designs using the circuit simulation models that are fitted to the final device metric values. The final integrated circuit can then be fabricated with the finalized process (**556**).

Referring now to FIG. **6**, a method of designing an integrated circuit according to another embodiment is shown in a flow diagram and designated by the general reference character **660**.

A method **660** can include creating an architectural representation of an integrated circuit (or portion thereof) in a higher level form. In the method of FIG. **6**, the integrated circuit can be instantiated in a high level block schematic form and further described in a higher level design language (**664**).

A method **660** can also include generating a more detailed (i.e., lower level) representation of the design described by interconnected circuit blocks. In FIG. **6**, this step can include generating a netlist (step **666**). Such a netlist can include higher order representations of circuit blocks interconnected to one another by nets.

Method **660** can also include generating device metric values (**626**) for each of the components of the netlist using statistical variation of process parameters, preferably according to any of the embodiments described herein. Circuit simulation models (SPICE) can then be created from such device metric values (**608**). The device metric values can be input a transistor simulation tool such as TCAD, to derive a set of structural and process parameters for the associated transistor device. Then, the appropriate adjustments could be made to the transistor design, for instance, longer gate length, or higher dose of implanted material to set threshold voltage. The result of starting with the device metric values can be an improved transistor design. Improved transistor design can be fed back into the method to derive an updated set of device metrics. The updated set of device metrics can be used to update the models for SPICE, by which updated simulations (**668**) of the circuits can be produced.

Referring now to FIG. **7**, one particular example of a netlist is shown in text form. A netlist **770** can include declarations of element types. In the particular example shown, element types can include nfet declarations **772** and pfet declarations **774**. Such elements (**772**/**774**) can have variables based on device metrics generated as shown in embodiments herein. In addition or alternatively, such elements can be processed by simulation software according to such device metrics.

Transistor types (e.g., **772**/**774**) can be conventional transistors, DDC transistors, or any other transistor types. A benefit of using a DDC transistor is, among other things, in the ability to pull in design corners and using the methods of the embodiments contemplated herein to refine the fabrication and create improved circuit simulation models.

FIG. **8**A shows a DDC type transistor **870** for which device metrics can be generated, according to embodiments. A DDC transistor **870** can be configured to have an enhanced body coefficient, along with the ability to set a threshold voltage (Vt) with enhanced precision. A DDC transistor **870** can include a gate electrode **882**, source **884**, drain **886**, and a gate dielectric **888** positioned over a substantially undoped channel **811**. Optional lightly doped source and drain extensions (SDE) **890** can be positioned respectively adjacent to source **884** and drain **886**. Such extensions **890** can extend toward each other, reducing effective length of the substantially undoped channel **811**.

In FIG. **8**A, the DDC transistor **870** is shown as an n-channel transistor having a source **884** and drain **886** made of n-type dopant material, formed upon a substrate such as a p-type doped silicon substrate providing a p-well **817**. In addition, the n-channel DDC transistor **870** in FIG. **8**A can include a highly doped screening region **815** made of p-type dopant material, and a threshold voltage set region **813** made of p-type dopant material.

Further descriptions of a DDC transistor as well as an exemplary fabrication process and other aspects of a DDC transistor can be found in U.S. Pat. No. 8,273,617, titled "Electronic Devices and Systems, and Methods for Making and Using the Same." A DDC transistor provides advantages for circuit design in that, among other reasons, a DDC transistor enables designs having pulled-in corners. The reason is the tighter distribution of the threshold voltage from device-to-device. Additionally, a DDC transistor includes a strong body coefficient by which body biasing can be used to further pull in design corners. A result of using a DDC transistor is the ability to implement improved integrated circuit designs according to desired targets for power and performance whereas when using conventional transistors circuit designers resort to designing conservatively for wider design corners thereby sacrificing the potential power and performance that could be otherwise achieved for a design. An advantage of using a DDC transistor as part of implementing on the embodiments described herein is in the ability to reliably design integrated circuits using a statistically-based, process variation-comprehending simulation model by which design corners could be shrunk.

FIG. **8**B shows a FinFET type transistor **870**-B for which device metrics can be generated, according to additional embodiments. The FinFET transistor **870**-B can include a gate electrode **882**-B and gate dielectric **888**-B that surround a substantially undoped channel **811**-B on opposing sides. The view of FIG. **8**B is taken along a channel length. Thus, it is understood that source and drain regions can extend into and out of the view shown.

FIG. **8**C shows a FinFET type transistor **870**-C having a screening region **815**-C, for which device metrics can be generated according to further embodiments. As in the case of FIG. **8**A, the FinFET transistor **870**-C has a screening region that can be configured to have an enhanced body coefficient, along with the ability to set a Vt with enhanced precision. The transistor **870**-C includes a gate electrode **882**-C and gate dielectric **888**-C formed over a substantially undoped channel **811**-C on opposing sides. However, unlike FIG. **8**B, a highly doped screening region **815**-C can be formed in a substrate **819** below substantially undoped channel **811**-C. Optionally, a Vt set region **813**-C can be formed between the screening region **815**-C and substantially undoped channel **811**-C.

As in the case of FIG. **8**B, the view of FIG. **8**C is taken along a channel length, and source and drain regions can extend into and out of the view, separated from screening region **815**-C by portions of undoped channel region **811**-C.

The geometries of transistor **870**-B can be the source of additional process source variations, not included for metrics of conventional transistors. Further, the geometries of transistor **870**-C, as well as the Vt set region and screening region, can be the subject of process source variations for metrics of such a transistor.

As noted above, the various methods and models according to embodiments can be utilized to generate device metrics for other transistor types (e.g., conventional MOSFETs, BJTs, JFETs, etc.).

It should be appreciated that in the foregoing description of exemplary embodiments of the invention, various features of the invention are sometimes grouped together in a single embodiment, figure, or description thereof for the purpose of streamlining the disclosure aiding in the understanding of one or more of the various inventive aspects. This method of disclosure, however, is not to be interpreted as reflecting an intention that the claimed invention requires more features than are expressly recited in each claim. Rather, as the following claims reflect, inventive aspects lie in less than all features of a single foregoing disclosed embodiment. Thus, the claims following the detailed description are hereby expressly incorporated into this detailed description, with each claim standing on its own as a separate embodiment of this invention.

It is also understood that the embodiments of the invention may be practiced in the absence of an element and/or step not specifically disclosed. That is, an inventive feature of the invention may be elimination of an element.

Accordingly, while the various aspects of the particular embodiments set forth herein have been described in detail, the present invention could be subject to various changes, substitutions, and alterations without departing from the spirit and scope of the invention.

What is claimed is:

1. A method, comprising:

assuming variation among process targets for a plurality of integrated circuit (IC) fabrication process sources of variation;

deriving relationships between each process source variance of the IC fabrication process and a device metric variance by operation of a computer program executed by a computer, the device metric variance being a variance in an IC performance characteristic;

generating a predicted device metric variation by at least multiplying each process source variation by the corresponding relationships between its process source variance and the device metric variance; and

designing at least a portion of an integrated circuit with the predicted device metric variation; wherein.

generating the predicted device metric variation includes calculating a root sum square of process source variations and the relationships between the corresponding process source variance and the device metric variance;

designing the at least a portion of the integrated circuit includes selecting process source variations having a greatest effect on the predicted device metric variation and creating a transistor performance model from at least the device metric; and

fabricating the at least a portion of the integrated circuit with the predicted device metric variation.

2. The method of claim **1**, wherein:

the relationships are generated from a semiconductor design automation tool executed by the computer.

3. The method of claim **2**, wherein:

the relationships are generated from a technology computer aided design (TCAD) automation tool.

4. The method of claim **1**, wherein:

the assumed variation values correspond to an IC fabrication process still under development.

5. A method, comprising:

assuming variation among process targets for a plurality of integrated circuit (IC) fabrication process sources of variation;

deriving relationships between each process source variance of the I C fabrication process and a device metric variance by operation of a computer program executed by a computer, the device metric variance being a variance in an I C performance characteristic;

generating a predicted device metric variation by at least multiplying each process source variation by the corresponding relationships between its process source variance and the device metric variance; and

designing at least a portion of an integrated circuit with the predicted device metric variation; wherein

generating the predicted device metric variation includes generating a device metric distribution from process source variation distributions and the relationships between the corresponding process source variance and the device metric variance;

designing the at least a portion of the integrated circuit includes any selected from the group consisting of: deriving correlations between device metrics and deriving correlations between device types; and

fabricating the at least a portion of the integrated circuit with the predicted device metric variation.

6. The method of claim **5**, wherein:

the relationships are generated from a semiconductor design automation tool executed by the computer.

7. The method of claim **6**, wherein:

the relationships are generated from a technology computer aided design (TCAD) automation tool.

8. The method of claim **5**, wherein:

the assumed variation values correspond to an IC fabrication process still under development.

9. A method, comprising:

assuming variation among process targets for a plurality of integrated circuit (IC) fabrication process sources of variation;

deriving relationships between each process source variance of the IC fabrication process and a device metric variance by operation of a computer program executed by a computer, the device metric variance being a variance in an IC performance characteristic;

generating a predicted device metric variation by at least multiplying each process source variation by the corresponding relationships between its process source variance and the device metric variance; and

designing at least a portion of an integrated circuit with the predicted device metric variation; wherein

generating the predicted device metric variation includes generating a corner device metric corresponding to corner process

source values, the corner process source values corresponding to an extreme end of a range of possible process source values;

designing the at least a portion of the integrated circuit includes designing a transistor model with at least the corner device metric; and

fabricating the at least a portion of the integrated circuit with the predicted device metric variation.

10. The method of claim **9**, wherein:

the relationships are generated from a semiconductor design automation tool executed by the computer.

11. The method of claim **10**, wherein:

the relationships are generated from a technology computer aided design (TCAD) automation tool.

12. The method of claim **9**, wherein:

the assumed variation values correspond to an IC fabrication process still under development.

* * * * *